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Design of PTL based Area Efficient and Low Power 4-bit ALU

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Abstract: Now a day's Area, Low power, and Speed are the major concerns of the VLSI circuits. In this paper a new design approach is introduced for reducing number of transistors and power consumption and dissipation in VLSI circuits. Here, a new design approach is followed based on pass transistor logic which provides better performance in terms of low power, area, and speed of the VLSI circuits. The explored method is implemented on ALU (Arithmetic Logic Unit) to reduce the trade off parameters. After compare the results of proposed ALU with conventional ALU, this Proposed ALU gives better performance in terms of power and area. All the work has been carried out on Tanner EDA Tool 13.0 and Micro wind 3.1.

Keywords: Pass Transistor Logic, Arithmetic Logic Unit, Low Power, Area.

I. INTRODUCTION

Recent years have witnessed tremendous advancement of portable electronic devices powered by batteries with intensive computational capabilities. The power requirements of these devices have increase in complexity of ICs because increased many folds. Now-a-days Area, low power, speed is major concerns of the VLSI circuit. Now-a-days logic circuits are designed using pass transistor logic (PTL) [1].

The proposed technique pass transistors logic use to design circuits have save power, increases speed and reduce area. This decreases complexity of ICs. The proposed technique used to design ALU at minimum number of transistors. In this ALU performs different logical and arithmetic operations. The pass transistor logic circuit should have the following features:

- Use minimum number of transistors
- Eliminating redundant transistors so reduce area.

II. ARCHITECTURE OF THE ALU

Mathematician John von Neumann was proposed in 1945 the ALU concept in a report on the foundations for a new computer called the EDVAC (Electronic Discrete Variable Automatic Computer) [2].The ALU is the part of the Central Processing unit which performs operations such as addition, subtraction and multiplication of integers and bit-wise AND, OR, NOT, XOR and other Boolean operations. This is in contrast to a floating-point unit (FPU), which operates on floating point numbers.

It is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units. A single CPU, FPU or GPU may contain multiple ALUs.

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logic function.

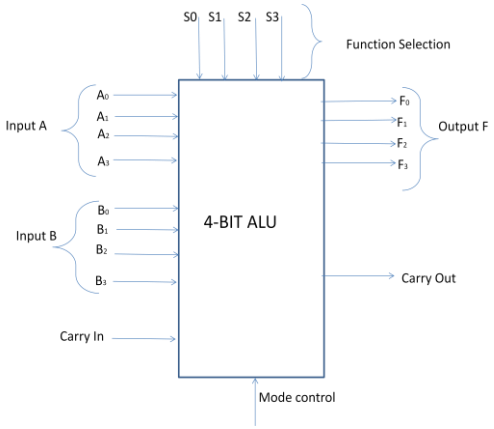

Fig.1. Block Diagram of ALU

The types of gates available are the NOT, AND, OR, NAND, NOR, EX-OR and EX-NOR. Except for the EX-NOR gate, are they available in monolithic integrated circuit form. The gate is a digital circuit with one or more input voltages but only one output voltage.

A. MUX:

Multiplexer also called MUX or a data selector is a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output. The routing of the desired data input to the output is controlled by 'SELECT' inputs. Normally there are 2^n input lines and n selection lines and one output whose bit combinations determine which input is selected.

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B. 2X1-MUX:

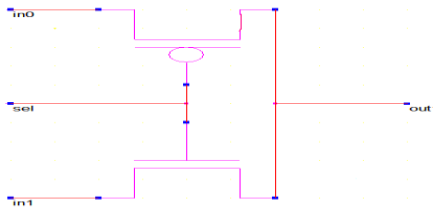

Fig.2. Basic View Of 2-T Mux

To shown above fig.2. The basic structure of the 2:1 mux[3] using pass transistor logic. In this mux have PMOS and NMOS along with selection line(sel) as shown above fig.2. The configuration of mux have PMOS works on ACTIVE LOW and NMOS works on ACTIVE HIGH. So the selection line (sel) is active low i.e '0' in the case PMOS activacted the resultant ouput is input of IN0. Similarly the selection line(sel) is active high i.e '1'in the case NMOS activacted the resultant output is input of IN1. Thus this circuitry behaves as a 2:1MUX with SEL-LINE selecting the favorable input for the output.

C . 2T-AND GATE

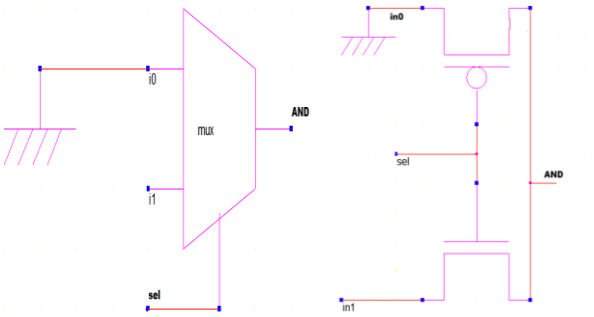

Fig.3. 2-T AND using 2-T MUX

The AND[3] gate implemented by the 2-trasistors usig 2-t mux as show above fig.3. AND gate have the output is high only when all inputs are high. The MUX using AND gate act as Selection line (SEL) is '0' or low then IN_0 or I_0 will be selected to the output. So the input IN_0 or I_0 is grounded, though put is always remaining at low state. Another side when selection line (l) is '1' i.e. High IN_1 or I_1 is selected. So the output will be either at low or high state following the AND gate as shown above fig.3.

D. 2-T OR GATE:

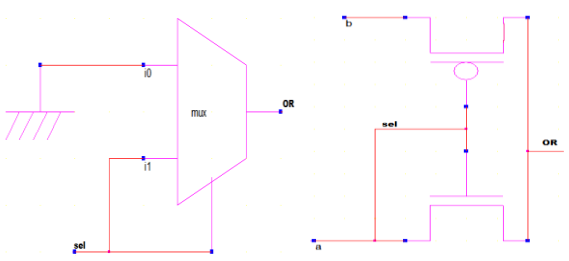

Fig.4.2-T OR gate using 2-T MUX

The OR [3] gate implemented by the 2-trasistors usig 2-t mux as show above fig.4. OR gate have the output is high when any of the inputs is high. The MUX using OR gate act as the input I_0 or B is always connected to ground and another input I_1 or A is connected to selection line (SEL). The selection line (SEL) is '0'or low. The output will be '0'. The selection line is '1' the output will be '1'or high. Shown the OR gate above fig.4.

E. 3-T XOR GATE:

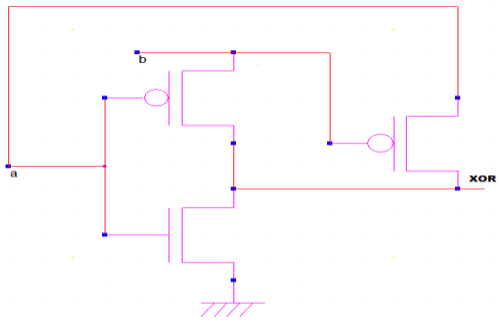

Fig.5.3-T XOR GATE

The XOR[3] gate act as the output is high only when odd number of inputs are high. The XOR [5] gate is design use 3-transistors i.e. 2-PMOS transistors and 1-NMOS transistor. The design is based on pass transistor logic. As shown above fig.5.

F. HALF ADDER:

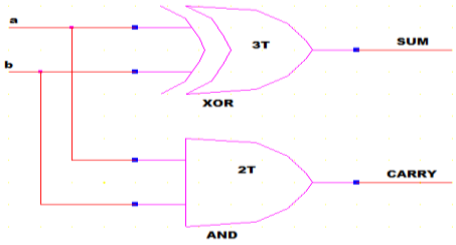

Fig.6. 5-T HALF ADDER

A combinational circuit that performs the addition of two bits is called a Half Adder [5]. The half adder designed using 5-transistor based on pass transistor logic. This design has 3-transistors XOR and 2-transistors AND gate. As shown above 5-T HALF ADDER fig.6.

G .FULL ADDER:

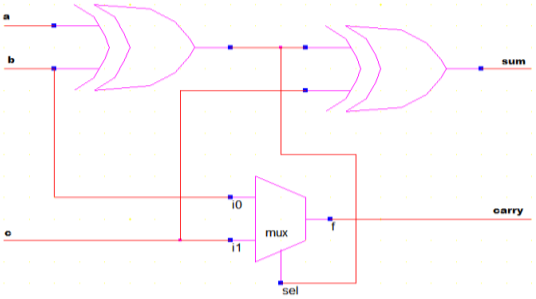

Fig.7.8-T FULL ADDER

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A Full adder [5] is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs and two outputs they are sum and carry. The full adder designed using 8-transistors based on pass transistor logic. In this circuit have 3-transistors XOR and 2-transistors AND gate and 2-transistors MUX. As shown above fig.7.

III. EXISTING METHOD

More no.of transistors are used to design conventional CMOS [3] ALU. I.e. The conventional CMOS ALU design use logic gates are AND gates have use 6-tansistors, OR gate have use 6-tansistors, XOR gate have use 12-tansistors ect. More number of transistors used conventional CMOS ALU, increases the area, reduce the speed, increases delay, and more power consumption.

IV. PROPOSED TECHNIQUE

4-BIT ALU:
Area, Low Power, Speed are major concerns of the VLSI circuit. So in this paper different operations like arithmetic and logical operations perform ALU [4]. An Arithmetic logic unit (ALU) is a digital electronic circuit that performs arithmetic and bitwise logical operations on integer binary numbers. The Design is minimum number of transistors used to design a 4-bit ALU. Comparison of proposed technique and conventional CMOS [3] ALU.

Measure the both techniques performance of – Area, no.of transistor count, Power consumption. The proposed design of 4-bit ALU basic building block as show fig.8.

In this have use multiplexers and logic gates and full adder. It's performing the mode control based logic and arithmetic operations. In this1st stage of 1-bit ALU have 8x1 MUX connected 8-operations and this output is connected to 2x1mux and another input is B_0.

The output of 2x1 MUX is connected to full-adder another inputs of full-adder is A and C_{in}. The outputs are sum and carry. Next stage of 8x1 mux has connected 8-other operations. This output is connected 2x1mux; another input is full-adder output sum.

The 2x1 MUX outcome of ALU result. So complete 1-bit ALU similarly the 4-bit ALU design is the 1-bit ALU carry is connected 2-bit ALU C_{in} i.e. C1.Similarly connected 2-bit to 3-bit and 3-bit to 4-bit ALU this are C2,C3. The total operation of 4-bit ALU as shown as fig.8.given below. The each bit performs the operations based on the mode-control. The mode-control zero-logical and one-arithmetic.

The 4-bit ALU in each bit perform the 16-operations. It have 4-selection lines, in this s3 act as mode control .The selection line s3 is zero(0) it performs the logic operations and s3 is one(1) it performs the arithmetic operation as show the truth table-I.

The 4-bit ALU designed used pass transistor logic so minimum number of transistors with design of 4-bit ALU. It's perform better compare to conventional CMOS 4-bit ALU. The better performs of Area and Power.

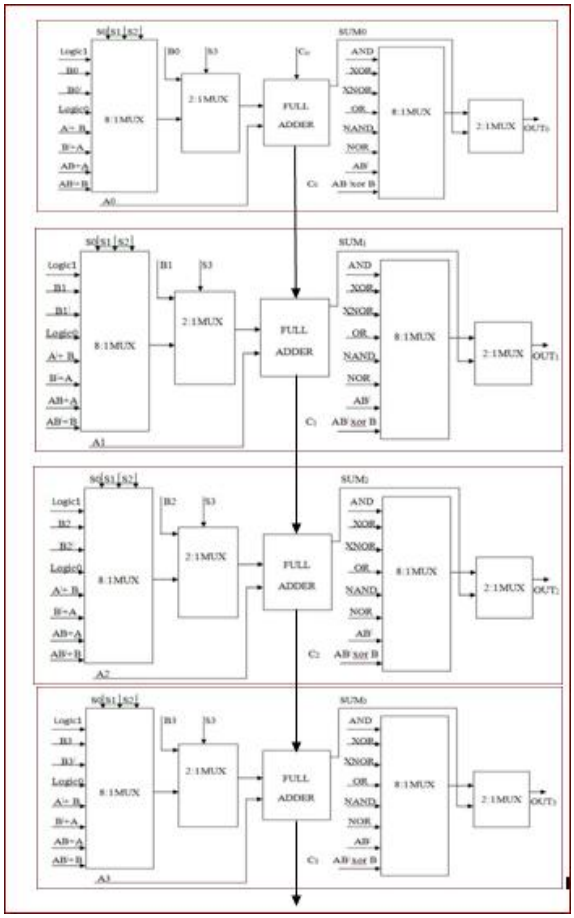

Fig.8: 4-bit ALU block diagram

TABLE I. Truth Table of ALU

S3	S2	S1	S0	Operations
0	0	0	0	AND
0	0	0	1	EXOR
0	0	1	0	EXNOR
0	0	1	1	OR
0	1	0	0	NAND
0	1	0	1	NOR
0	1	1	0	A'B
0	1	1	1	A'B XOR B
1	0	0	0	ADDITION
1	0	0	1	SUBTRACTION
1	0	1	0	INCREMENT
1	0	1	1	DECREMENT
1	1	0	0	A'+B XOR A XOR C
1	1	0	1	A+B'XOR AXOR C
1	1	1	0	AB+A XOR A XOR C
1	1	1	1	AB'+ B XOR A XOR C

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TABLE II. Comparison Table

S.NO:	parameters	Number Of Transistors	
		Pass Transistor Logic (PTL)	Conventional CMOS logic
1.	AND	2	6
2.	OR	2	6
3.	XOR	3	12
4.	XNOR	5	12
5.	NAND	4	8
6.	NOR	4	8
7.	FULL-ADDER	8	42
8.	1-BIT-ALU	91	478

V. SIMULATION RESULTS

The design of 4-bit ALU in the part of 1-bit ALU is design gate and transistor level in micro wind tool. This tool is used only for simulation analysis purpose. The performance analysis purpose used for Tanner EDA Tool Micro Wind Results:

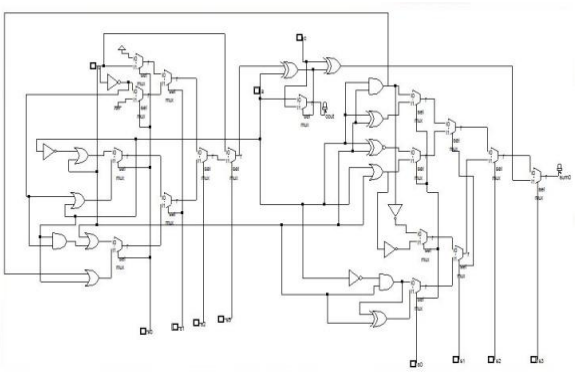

Fig.9: Simulation Result of Gate Level Design of 1-Bit ALU

Transistor level design of 1-bit ALU

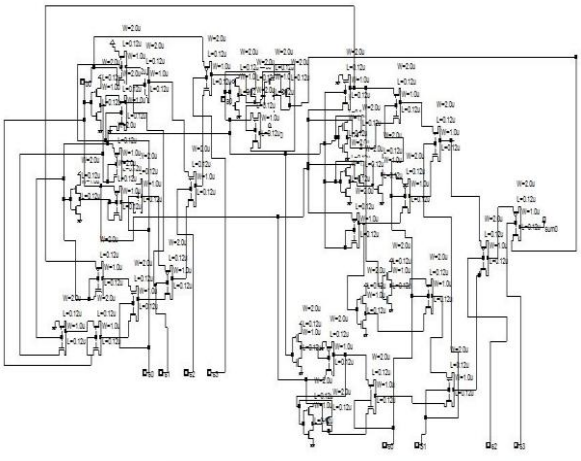

Fig.10: Simulation Result of Transistor Level Design of 1-Bit ALU

Tanner EDA Tool Results:
1-bit ALU

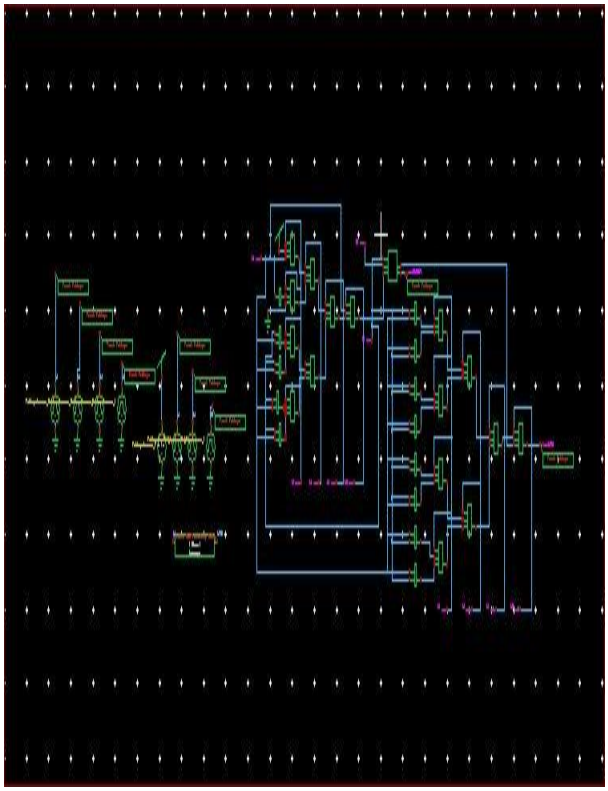

Fig.11:1-Bit ALU

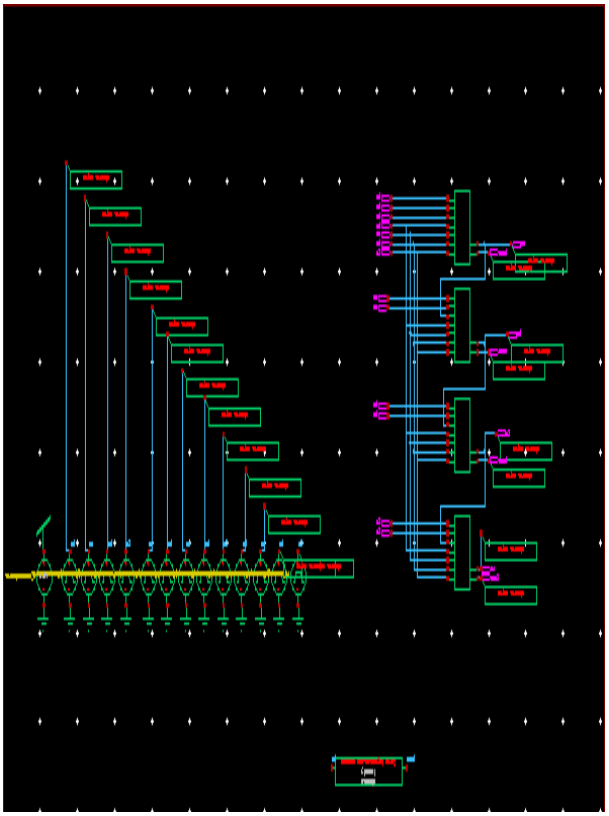

Fig.12: 4-Bit ALU

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Proposed 4-Bit ALU Wave Forms:

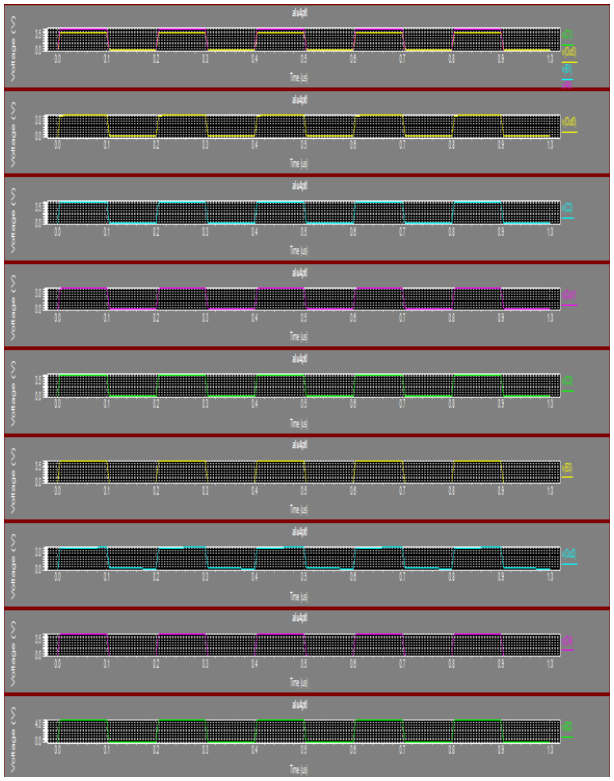

Fig.13: Proposed 4-Bit ALU Wave Forms

Conventional CMOS 4-bit ALU Wave forms:

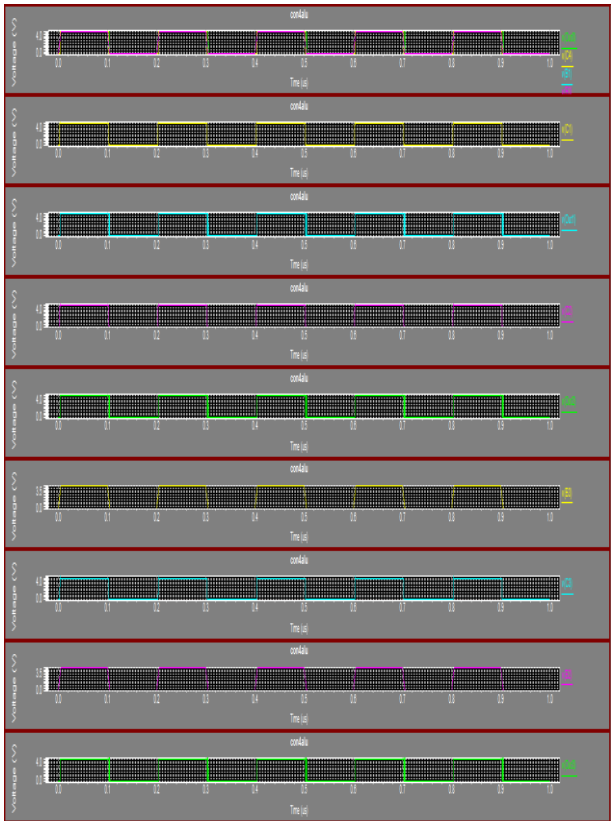

Fig.14: Conventional CMOS 4-bit ALU Wave forms

VI. COMPARISONS

The comparison of pass transistor logic (PTL) and Conventional CMOS logic. The both performance analysis of 4-BIT ALU based on Tanner EDA tool .The results as show in comparison table-III.

TABLE III. Comparison Table

S. NO	Parameters	Pass Transistor Logic (PTL)	Conventional CMOS logic
		4-bit ALU	4-bit ALU
1.	Number of Transistors	364	1912
2.	Power Consumption (watts)	2.582140e-002	1.203783e-001
3.	Maximum Power (Watts)	3.284747e-002	2.421613e-001
4.	Minimum Power (Watts)	1.879532e-002	1.404702e-001
5.	Tran_ measure_ delay(S)	4.6047e-010	8.6267e-010

VII. CONCLUSION

In this project designed proposed 4-bit ALU based on PTL (pass transistor logic). The designed 4-bit ALU gate level and transistor level in Micro wind tool it is use for simulation purpose. The performance analysis measured Tanner EDA tool. Measured the comparison of proposed and conventional CMOS ALU. The performance of – no. of Transistor count, Power Consumption, Delay. In this better performance of results the PTL, because transistor count is reduce compare to conventional CMOS ALU and power is also better than conventional CMOS ALU.

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